

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended) A method for planarizing of fabricating an MRAM cell structure ~~on an MRAM chip having an insulation layer with an uneven top surface formed on an~~ ~~a plurality of MTJ elements which is comprised of a bottom layer on a substrate, a free layer on the bottom layer, and a each with an uppermost cap layer that has a certain thickness on the free layer whereby the certain thickness is controlled within a range of about +/- 5 Angstroms,~~ comprising:

(a) providing a plurality of MTJ elements on a substrate and depositing an insulation layer on the substrate to a level that covers the MTJ elements including a top surface of said cap layer;

(a)(b) performing a CMP step to planarize said insulation layer wherein the planarized insulation layer has a certain first thickness above the top surface of said cap layer; and

(b)(c) performing an etch back step to reduce the thickness of said insulation layer wherein the insulation layer is planarized at a certain second thickness below the top surface of said cap layer.

Claim 2 (original) The method of claim 1 wherein the insulation layer is comprised of silicon oxide or a low k dielectric material and has a thickness of about 800 to 2000 Angstroms above said cap layer before said CMP step.

Claim 3 (original) The method of claim 1 wherein said certain thickness above the cap layer is about 60 to 200 Angstroms.

Claim 4 (currently amended) The method of claim 1 wherein said certain second thickness below the top surface of said cap layer is about 50 to 190 Angstroms.

Claim 5 (original) The method of claim 1 wherein the cap layer is comprised of Cu, Ru, or a composite layer with an upper Ru layer.

Claim 6 (currently amended) The method of claim 5 wherein the cap layer has a certain thickness that is reduced by less than 5 Angstroms during said etch back step.

Claim 7 (original) The method of claim 1 wherein etch back step is a plasma etch based on a fluorocarbon chemistry that has a high selectivity between the insulation layer and said cap layer.

Claim 8 was cancelled.

Claim 9 (currently amended) The method of claim 1 wherein said MRAM chip is further comprised of a plurality of MTJs that have a cap layer thickness variation of less than +/- 5 Angstroms after the etch back step first thickness is about 250 Angstroms greater than said second thickness.

Claim 10 (currently amended) The method of claim 9 1 wherein the certain thickness of said cap layer thickness is between about 50 and 400 Angstroms.

Claim 11 (currently amended) A method for fabricating an MRAM cell structure on an MRAM chip having a plurality of MTJ elements each with an uppermost cap layer that has a certain thickness whereby the certain thickness is controlled within a range of about +/- 5 Angstroms, comprising:

- (a) forming a first conductive layer comprised of a first line on a substrate;
- (b) forming an a plurality of MTJ elements on said first line, said each MTJ has having a bottom layer, a free layer on said bottom layer, and a cap layer on said free layer;
- (c) depositing an insulation layer on said MTJ and on said substrate to a level that covers the MTJ elements including a top surface of said cap layer;
- (d) performing a CMP step to planarize said insulation layer wherein the planarized insulation layer a certain first thickness above the top surface of said cap layer;
- (e) performing an etch back step to reduce the thickness of said insulation layer wherein the insulation layer is planarized at a certain second thickness below the top surface of said cap layer; and
- (f) forming a second conductive layer on said insulation layer and cap layer, said second conductive layer is comprised of a second line that contacts the top surface of said cap layer.

Claim 12 (currently amended) The method of claim 11 wherein the bottom layer of said MTJ elements is a composite layer comprised of a seed layer on said first line, an AFM layer on the seed layer, a pinned layer on the AFM layer, and a tunnel barrier layer on the pinned layer.

Claim 13 (original) The method of claim **11** wherein the first line is comprised of copper and is a bottom electrode, a bit line, or a word line.

Claim 14 (original) The method of claim **11** wherein the second line is comprised of copper and is a word line or bit line.

Claim 15 (currently amended) The method of claim **11** wherein said certain first thickness above the cap layer is about 60 to 200 Angstroms.

Claim 16 (currently amended) The method of claim **11** wherein said certain second thickness below the cap layer is about 50 to 190 Angstroms.

Claim 17 (original) The method of claim **11** wherein the cap layer has a thickness between about 50 and 400 Angstroms and is comprised of Cu, Ru, or a composite layer with an upper Ru layer.

Claim 18 (original) The method of claim **17** wherein said cap layer has a thickness that is reduced by less than 5 Angstroms during said etch back step.

Claim 19 (currently amended) The method of claim **11** wherein the MTJ elements has have a width from about 0.2 to 0.9 microns.

Claim 20 (original) The method of claim **11** wherein the insulation layer is comprised of silicon oxide or a low k dielectric material and has a thickness of about 800 to 2000 Angstroms above said cap layer before said CMP step.

Claim 21 (original) The method of claim **11** wherein etch back step is a plasma etch based on a fluorocarbon chemistry that has a high selectivity between the insulation layer and said cap layer.

Claim 22 was cancelled.

Claim 23 (original) The method of claim **11** wherein said MRAM chip is further comprised of a plurality of MRAM cells that have a distance variation of less than +/- 5 Angstroms from a free layer to an overlying second line after the etch back step.

Claim 24 (original) The method of claim **11** wherein the MRAM chip is further comprised of an array of lines in said first conductive layer that are parallel to said first line, an array of lines in the second conductive layer that are parallel to the second line, and an array of MTJs formed at each location where a second line crosses over a first line wherein the distance between a free layer and an overlying second line is maintained to within 10 Angstroms.

Claims 25 to 34 are cancelled.